Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
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L2	4	(("4385278") or ("4777618") or ("5954782") or ("5808921")).PN.	US-PGPUB; USPAT	OR	OFF	2005/01/31 12:02
L3	105	703/7.ccor.	US-PGPUB; USPAT	OR	ON	2005/01/31 12:02
L4	291	703/13.ccor.	US-PGPUB; USPAT	OR	ON	2005/01/31 12:02
L5	94	703/19.ccor.	US-PGPUB; USPAT	OR	ON	2005/01/31 12:02
L6	1272	hardware near3 loop	US-PGPUB; USPAT	OR	ON	2005/01/31 12:02
L7	143	L6 same simulation	US-PGPUB; USPAT	OR	ON	2005/01/31 12:02
L8	83	L7 and fpga	US-PGPUB; USPAT	OR	ON	2005/01/31 12:02
L9	3	L8 and @ad<="19990831"	US-PGPUB; USPAT	OR	ON	2005/01/31 12:02
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L11	7	L10 and @ad<="19990831"	US-PGPUB; USPAT	OR	ON	2005/01/31 12:02
L12	3557	asynchronous same sampl$4	US-PGPUB; USPAT	OR	ON	2005/01/31 12:02
L13	1373	L12 and programmable	US-PGPUB; USPAT	OR	ON	2005/01/31 12:02
L14	816	L13 and @ad<="19990831"	US-PGPUB; USPAT	OR	ON	2005/01/31 12:02
L15	119	L14 and simulation	US-PGPUB; USPAT	OR	ON	2005/01/31 12:02
L16	96	L15 and (processor microprocessor)	US-PGPUB; USPAT	OR	ON	2005/01/31 12:02
L17	2	("4777618").URPN.	USPAT	OR	ON	2005/01/31 12:02
L18	1	("6646397").PN.	US-PGPUB; USPAT	OR	OFF	2005/01/31 12:02
L19	139	hardware-in-the-loop	US-PGPUB; USPAT	OR	ON	2005/01/31 12:02
L20	83	L19 and fpga	US-PGPUB; USPAT	OR	ON	2005/01/31 12:02
L21	1	L20 and @ad<="19990831"	US-PGPUB; USPAT	OR	ON	2005/01/31 12:02
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L23	9	("5166592" | "5220259" | "5355060" | "5473230" | "5677611" | "5734242" | "5912539" | "6014598" | "6330140").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2005/01/31 12:02
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2 Active pages: a computation model for intelligent memory
Mark Oskin, Frederic T. Chong, Timothy Sherwood
April 1998 **ACM SIGARCH Computer Architecture News , Proceedings of the 25th annual international symposium on Computer architecture**, Volume 26 Issue 3
Full text available: pdf(1.58 MB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

3 An SBus monitor board
H. A. Xie, K. E. Forward, K. M. Adams, D. Leask
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4 Virtual chip: making functional models work on real target systems
Namseung Kim, Hoon Choi, Seungjong Lee, Seungwang Lee, In-Cheolo Park, Chong-Min Kyung
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5 Design methodology of a 200MHz superscalar microprocessor: SH-4
Toshihiro Hattori, Yusuke Nitta, Mitsuho Seki, Susumu Narita, Kunio Uchiyama, Tsuyoshi Takahashi, Ryuichi Satomura
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Full text available: pdf(282.85 KB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

6 Analysis of unconventional evolved electronics
Adrian Thompson, Paul Layzell
April 1999 **Communications of the ACM**, Volume 42 Issue 4
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7 Performance optimization of wireless local area networks through VLSI data compression
Bongjin Jung, Wayne P. Burleson
January 1998 **Wireless Networks**, Volume 4 Issue 1
Full text available: pdf(664.69 KB) Additional Information: full citation, abstract, references, citings, index terms

8 Robust FPGA intellectual property protection through multiple small watermarks
John Lach, William H. Mangione-Smith, Miodrag Potkonjak
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Full text available: pdf(119.08 KB) Additional Information: full citation, references, citings, index terms

9 String matching on multicontext FPGAs using self-reconfiguration
Reetinder P. S. Sidhu, Alessandro Mei, Viktor K. Prasanna
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10 ATM traffic shaper: ATS
J. C. Diaz, P. Plaza, J. Crespo
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Full text available: pdf(417.61 KB) Publisher Site Additional Information: full citation, abstract, references, index terms

11 Functional verification methodology of Chameleon processor
Françoise Casaubieilh, Anthony McIsaac, Mike Benjamin, Mike Bartley, François Pogodalla, Frédéric Rocheteau, Mohamed Belhadj, Jeremy Eggleton, Gérard Mas, Geoff Barrett, Christian Berthet
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12 A hardware/software prototyping environment for dynamically reconfigurable embedded systems
Josef Fleischmann, Klaus Buchenrieder, Rainer Kress
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Full text available: pdf(42.66 KB) Publisher Site Additional Information: full citation, references, citings, index terms

13 A timing driven N-way chip and multi-chip partitioner
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14 Clock skew optimization for ground bounce control
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15 Interface timing verification drives system design
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16 Exploration of hardware/software design space through a codesign of robot arm controller
M. Abid, A. Changuel, A. Jerraya
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17 Instruction set selection for ASIP design
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18 An extendable MIPS-I processor kernel in VHDL for hardware/software co-design
M. Gschwind, D. Maurer

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19 Breakpoints and breakpoint detection in source-level emulation

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François Clouté, Jean-Noël Contensou, Daniel Esteve, Pascal Pampagnin, Philippe Pons, Yves Favard

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Paul Lippens, Vijay Nagasamy, Wayne Wolf

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Alexandro M. S. Adário, Eduardo L. Roehe, Sergio Bampi

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25 Profiling in the ASP codesign environment

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27 Reducing TLB and memory overhead using online superpage promotion

Theodore H. Romer, Wayne H. Ohlrich, Anna R. Karlin, Brian N. Bershad

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28 The DASH prototype: implementation and performance

Daniel Lenoski, James Laudon, Truman Joe, David Nakahira, Luis Stevens, Anoop Gupta, John Hennessy
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29 Transformational partitioning for co-design of multiprocessor systems
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30 The practical application of retiming to the design of high-performance systems
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31 Design and implementation of a prototype optical deflection network
John Feehrer, Jon Sauer, Lars Ramfelt
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33 Intellectual property re-use in embedded system co-design: an industrial case study
E. Filippi, L. Lavagno, L. Licciardi, A. Montanaro, M. Paolini, R. Passerone, M. Sgroi, A. Sangiovanni-Vincentelli
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34 PSCP: a scalable parallel ASIP architecture for reactive systems
A. Pyttel, A. Sedlmeier, C. Veith
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35 A 50-Gb/s IP router
Craig Partridge, Philip P. Carvey, Ed Burgess, Isidro Castineyra, Tom Clarke, Lise Graham, Michael Hathaway, Phil Herman, Allen King, Steve Kohalmi, Tracy Ma, John Mcallen, Trevor Mendez, Walter C. Milliken, Ronald Pettyjohn, John Rokosz, Joshua Seeger, Michael Sollins, Steve Storch, Benjamin Tober, Gregory D. Troxel
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36 Hardware-software-codesign of application specific microcontrollers with the ASM environment
A. Both, B. Biermann, R. Lerch, Y. Manoli, K. Sievert
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37 Hardware/software co-design of a fuzzy RISC processor
V. Salapura, M. Gschwind
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38 PARAS: system-level concurrent partitioning and scheduling
Wing Hang Wong, Rajiv Jain

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Control Systems Technology, IEEE Transactions on , Volume: 7 , Issue: 6 , Nov. 1999
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[Abstract] [PDF Full-Text (196 KB)] IEEE JNL

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2 **Sliding mode input-output linearization and field orientation for real-time control of induction motors**
Benchaib, A.; Rachid, A.; Audrezet, E.;
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Pages:3 - 13

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3 **The formulation and implementation of an analog/digital control system for a 100-kW dc-to-dc buck chopper**
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Coakley, N.G.; Kavanagh, R.C.;
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Benchaib, A.; Rachid, A.; Audrezet, E.; Tadjine, M.;
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Kavanagh, R.C.; Murphy, J.M.D.;
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Dmitriev-Zdorov, V.B.;
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11 **Fault tolerance via weight noise in analog VLSI implementations of MLPs-a case study with EPSILON**
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Mi-Ching Tsai; Chung-Chi Chou; Min-Fu Hsieh;
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Wagner, J.R.; Keane, J.F.;
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16 **Long haul participation in a distributed interactive simulation demonstration**
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18 **An integrated approach to feature based dynamic vision**
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Powers, W.;
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Van Campenhout, J.; Van Marck, H.; Depreitere, J.; Dambre, J.;
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Chow, P.; Soon Ong Seo; Rose, J.; Chung, K.; Paez-Monzon, G.; Rahardja, I.;
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Shih-Liang Jung; Meng-Yueh Chang; Jin-Yi Jyang; Li-Chia Yeh; Ying-Yu Tzou;
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Pages:522 - 532

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[Abstract] [PDF Full-Text (204 KB)] IEEE JNL

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Funabiki, N.; Yoda, M.; Kitamichi, J.; Nishikawa, S.;
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Hamblen, J.O.; Owen, H.L.; Yalamanchili, S.; Binh Dao;
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Pages:8 - 14

[Abstract] [PDF Full-Text (112 KB)] IEEE JNL

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Pages:6 - 23

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17 **Dynamic algorithm transformations (DAT)-a systematic approach to low-power reconfigurable signal processing**
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[Abstract] [PDF Full-Text (316 KB)] IEEE JNL

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Yao, X.; Higuchi, T.;
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Welch, J.T.;
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McKenzie, N.R.; Ebeling, C.; McMurchie, L.; Borriello, G.;
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Babb, J.; Tessier, R.; Dahl, M.; Hanono, S.Z.; Hoki, D.M.; Agarwal, A.;
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The Chinook Hardware/Software Co-Synthesis System - Chou, Ortega, Borriello (1995) (Correct) (18 citations)
circuits including **microprocessors**, **programmable logic**, and devices such as LCDs, network **processors** and/or custom logic and the co-**simulation** of system specifications before, during, and are applied to a window of data samples. Digital **signal** processing (DSP) systems are the canonical
ftp.cs.washington.edu/tr/1995/03/UW-CSE-95-03-04.PS.Z

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Run-Time Compaction of FPGA Designs - Diessel, ElGindy (1997) (Correct) (11 citations)
Y. K. Cheung, and M. Glesner, editors, Field-**Programmable Logic** and Applications, 7th International bit-streams with new offsets. We show by **simulation** that significant performance improvements are at least one order of magnitude greater than the **signal** delay of a cell or the latency of a wire. We
ftp.cs.newcastle.edu.au/pub/techreports/tr97-02.ps.Z

A Compiler for Application-Specific Signal Processors - Rimey, Hilfinger (1988) (Correct) (10 citations)
it is actually a state machine based on a **programmable logic** array, it can simultaneously evaluate any not strictly compatible with C. For behavioral **simulation**, we provide a translator that converts RL into A Compiler for Application-Specific **Signal Processors** Ken Rimey and Paul N. Hilfinger
www.cs.hut.fi/~rimey/papers/monterey/paper.ps

Increasing Microprocessor Performance with.. - Sawitzki, Gratz, Spallek (1998) (Correct) (8 citations)
microprocessor cores with tightly-coupled **programmable logic** started to appear [7-9]In this paper we and reconfigurable logic on the same die. **Simulations** have shown that even a comparatively simple be easily scaled. The **simulation** of the critical **signal** path within CoMPARE indicates that the 8-bit
www.inf.tu-dresden.de/~ss9/fpl98.ps.gz

Cameron: High Level Language Compilation for.. - Hammes, Rinker.. (1999) (Correct) (7 citations)
based on FPGAs, which are large arrays of **programmable logic** cells, organized into one or more arrays of code and FPGA configurations. The compilation, **simulation** and execution path, shown in figure 1, uses and Hutchings specifically consider digital **signal** processing tasks, and also calculate a ten-fold
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ASOC: A Scalable, Single-Chip Communications Architecture - Liang, Swaminathan, Tessier (2000) (Correct) (2 citations)
Corporation, integrates a microcontroller, **programmable logic**, and a number of peripherals (UART, SoC interconnect architectures via parallel **simulation**. Additionally, a preliminary layout of our attributed to two factors: capacitive off-chip **signal** delays and a need for growing numbers of
www.ecs.umass.edu/ece/tessier/courses/669/pact00.ps.gz

A Framework for Developing Parametrised FPGA Libraries - Luk Guo (1996) (Correct) (2 citations)
FastMap **processor** interface"in Field **Programmable Logic** and Applications, W. Moore and W. Luk Third, while some library generators provide **simulation** models for their circuits, there is no and adders increasingly complex libraries for **signal** processing and other applications are beginning
www.doc.ic.ac.uk/~wl/papers/fpl96.ps.gz

Simulation of Evolvable Hardware to Solve Low Level.. - Hollingworth.. (1999) (Correct) (1 citation)
Gate Array (FPGA)7] devices and **Programmable Logic** Devices (PLD)since these can be **Simulation** of Evolvable Hardware to Solve Low Level Image
filter, which is simple to implement on Digital **Signal Processor**(DSP) technology. The first step in
www.amp.york.ac.uk/external/media/cal/bio-insp/publications/gsh-evoiasp99.pdf

Using Large CPLDs and FPGAs for Prototyping and VGA Video.. - James Hamblen School (1999) (Correct) (1 citation)
tools and higher gate capacity CPLD, Complex **Programmable Logic** Device, and FPGA, Field Programmable Gate

to provide students with logic synthesis and **simulation** CAD tools and to provide low cost hardware using hardware inside the CPLD or FPGA. Only five **signals** or pins are required, two sync **signals** and www.ece.gatech.edu/users/hamblen/ALTERA/wcae98.PDF

An Array Architecture for Reconfigurable Datapaths - Wang, Gulak (1993) (Correct) (1 citation)
C =Carry Logic Block L L L Table Lookup **Programmable Logic** Box Programmable Routing Box Programmable examples are presented. The design modelling and **simulation** of the datapath using VHDL are described and we for a simple routing interconnection for control **signals**. Other features can be exploited in the design www.eecg.toronto.edu/~qiang/research/papers/paperOxford.ps

An Array Architecture for Reconfigurable Datapath - Wang (1998) (Correct) (1 citation)
Logic Block L L L Table Lookup Invertor **Programmable Logic** Box (a) The Programmble Routing and Logic sequence is used as a test vehicle in the **simulations**. Qiang Wang An Array Architecture for FPGAs to prototype **microprocessors** and digital **signal processors** of various types. An FPGA consists of www.eecg.toronto.edu/~qiang/research/theses/Mthesis.ps

The CPU Design Kit: An Instructional Prototyping Platform for.. - Anujan Varma (1995) (Correct) (1 citation)
be explored. With the availability of dense **programmable logic** chips such as the Altera FLEX series, it environment for design entry, synthesis, and **simulation** of the system from a high-level language the register file and caches, monitor the state of **signals** on the board, and control execution of the CPU. ftp.cse.ucsc.edu/pub/hsnlab/cpukit.ps.Z

Resume - Panchal (Correct)
Programming, testing and installation of **programmable logic** controllers (GE-Fanuc)B.E. Thesis work : A Methodology of Modeling Wireless Networks **Simulation** Advisors: Prof. Roy Yates and Prof. Andrew (B.E. thesis) The project is based on digital **signal** processing and artificial neural networks. www.caip.rutgers.edu/~jpanchal/resume/resume.ps

Design of Highly Parallel Edge Detection Nodes Using.. - Hollingworth, Smith.. (1999) (Correct)
gap to engineering, but with the advent of **programmable logic** devices, such as FPGAs, the interest of to the particular images encountered. The **simulation** of such a system through the use of be simple to implement (particularly on Digital **Signal Processor** (DSP) technology) and are particularly www.amp.york.ac.uk/external/media/cal/bio-insp/publications/gsh-pdp99.pdf

Unknown - (Correct)
main categories of FPDs: simple and complex **programmable logic** devices, and field-programmable gate Using Vhdl For Board Level **Simulation** Sandi Habinc European Space Agency Peter estimating transition probabilities of internal **signals** in combinational circuits uses Markov chains and www.iro.umontreal.ca/~aboulham/synthA97.pdf

A Concept for an Evaluation Framework for Reconfigurable Systems - Sawitzki, Spallek (1999) (Correct)
as a combination of hardwired and **programmable logic**. The coupling between these components is in the time-consuming development of dedicated **simulation** and prototyping environments, especially if the [8]A benchmark set consisting of three digital **signal** processing algorithms was run on a variety of www.inf.tu-dresden.de/~ss9/fpl99.ps.gz

High--Bandwidth Trace Collection for Multicomputer.. - Charles Hudnall (Correct)
probes to memory is implemented in **programmable logic**. Breakpoint-style debugging support is Research Center for Computational Field **Simulation** Mississippi State University Abstract is also provided via the SPInet Halt/Resume **signals**. The design of the SPIcontrol board is driven by www.erc.msstate.edu/thrusts/ca/html/../publications/SSSTSPIcontrol.ps.gz

Finite-Word-Length and Nonrecursive Implementation of.. - Fischer, Huber (1997) (Correct)
processor, but it is necessary to employ **programmable logic** devices (PLDs) or application specific input is described analytically. Examples and **simulation** results demonstrate the validity of these interest. Because, over the last decade, digital **signal** processing has made a big progress, high-rate www-nt.e-technik.uni-erlangen.de/~dcg/papers/aeu_97.ps.gz

Application of a TMS320C31 chip for DSP/Embedded System - Feng, Olsen, Pietraski.. (Correct)
In addition, the system has several **programmable logic** devices[5] to program the counting function facilitate computer **simulation**, debugging and embedded-system development. To

development on a fixed platform. TMS320C31 read **signal** write **signal** Active Buffer Pod SN74ACT8990 Test
adwww.fnal.gov/www/icalepcs/abstracts/Postscript/fpo46.ps

Flexible codesign target architecture for early.. - Tammemäe, O'Nils, Hemani (Correct)
of System Synthesis, ISSS'95. 12. The **Programmable Logic** Data Book"Xilinx, Inc.1994. 13. M.
from HW side, thus establishing real clock-level **simulation**. Coemulation. Hardware is programmed into FPGA
initialises selected function. After completion **signal** "done" can be polled out from server (HW) status
www.ele.kth.se/ESD/doc/ar96/nalle/springer.ps.gz

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with real-time issues, human-in-the-**loop** or **hardware**-in-the-**loop**. Whether a **simulation** is discrete
been concerned with real-time issues, human-in-the-**loop** or **hardware**-in-the-**loop**. Whether a **simulation** is
A Spectrum Of Options For Parallel **Simulation** Paul F. Reynolds, Jr. Ipc-Tr-88-007 Sept. 9,
ftp.cs.virginia.edu/pub/techreports/IPC-88-07.ps.Z

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SPECTRUM: A Parallel Simulation Testbed+ - Reynolds, Jr., Dickens (1989) (Correct) (5 citations)
with real-time issues, human-in-the-**loop** or **hardware**-in-the-**loop**. In [Reyn88] we showed that,
been concerned with real-time issues, human-in-the-**loop** or **hardware**-in-the-**loop**. In [Reyn88] we showed
Spectrum: A Parallel **Simulation** Testbed Paul F. Reynolds, Jr. Phillip M.
ftp.cs.virginia.edu/pub/techreports/IPC-89-12.ps.Z

Modeling And Realtime Simulation Of An Automatic Gearbox .. - Otter, Schlegel.. (1997) (Correct) (3 citations)
object oriented modeling, automatic gearbox, **hardware**-in-the-**loop simulation**, Modelica. ABSTRACT To
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Modeling And Realtime **Simulation** Of An Automatic Gearbox Using Modelica Martin
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A Step towards Operating System Synthesis - Ditze (1998) (Correct) (1 citation)
when considering design methodologies like **Hardware**-in-the-**Loop**: Starting with a pure (distributed)
embedded subsystems. Usually, a high-level control **loop** executes a large block of software instructions at
Starting With A Pure (distributed) **Simulation** The Entire System Requires A Distributed Hpc Os
www.uni-paderborn.de/sfb376/projects/b1/PS/Dit98a.ps.gz

Bruce E. Tucker - Kenneth Zabel Sparta (Correct)
by this computation is used as part of a **hardware**-in-the-**loop** (HWIL) RTTC test facility, which
computation is used as part of a **hardware**-in-the-**loop** (HWIL) RTTC test facility, which tests imaging
for a real-time **hardware**-in-the-**loop** (HWIL) **simulation** facility at the U.S. Army Redstone Technical
fly.hiwaay.net/~betucker/itea_paper.pdf

Modeling Of Hydraulic Systems For Hardware-In-The-Loop.. - Ferreira, al. (Correct)
Modeling Of Hydraulic Systems For **Hardware**-In-The-**Loop Simulation**: A Methodology Proposal
Modeling Of Hydraulic Systems For **Hardware**-In-The-**Loop Simulation**: A Methodology Proposal Jorge A.
Of Hydraulic Systems For **Hardware**-In-The-**Loop Simulation**: A Methodology Proposal Jorge A. Ferreira
www.modelica.org/papers/ASME_P.pdf

Comparative analysis between automatic design methodology and.. - Cilio (1996) (Correct)
. 10 2.1.3 **Hardware** subsystem .
cardit.et.tudelft.nl/MOVE/papers/cilio96.ps.gz

Real Time Simulation and Online Control for.. - Chucholowski.. (1999) (Correct)
must be performed in real time for application in **Hardware**-in-the-**Loop** experiments. Numerical results are
in real time for application in **Hardware**-in-the-**Loop** experiments. Numerical results are presented for
Real Time **Simulation** and Online Control for Virtual Test Drives of
www-m2.mathematik.tu-muenchen.de/~stryk/paper/1998-fortwihr-tesis.ps.gz

Hardware/software Co-Design For Dsp Applications Via The Hms.. - Michael Sheliga (Correct)
Hardware/software Co-Design For Dsp Applications Via The
algorithms for performing partitioning, scheduling, **loop** pipelining (retiming)**hardware** needability
the least design time. They also require less **simulation**, test and verification time. However,

www.nd.edu/~esha/papers/mike/hms_icassp4.ps